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A Self-Powered and Area Efficient SSHI Rectifier for Piezoelectric Harvesters

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ABSTRACT This article presents an area efficient fully autonomous piezoelectric energy harvesting system to scavenge energy from periodic vibrations. Extraction rectifier utilized in the system is based on synchronized switch harvesting on inductor (SSHI) technique which enables system to outperform standard passive rectifiers. Compared to conventional SSHI circuits, enhanced SSHI (E-SSHI) system proposed in this paper uses a single low-profile external inductor in the range of μH's to reduce overall system cost and volume, hence broadening application areas of such harvesting systems. Furthermore, E-SSHI does not include any negative voltage converter circuit and therefore, it offers area efficient AC/DC rectification. Detection of optimal voltage flipping times in E-SSHI technique is conducted autonomously without any external calibration. Energy transfer circuit provides control over how much energy is delivered from E-SSHI output to electronic load. The proposed system is fabricated in 180 nm CMOS process with 0.28 mm^2 active area. It is tested using a commercial piezoelectric transducer MIDE V22BL with periodic excitation. Measured results reveal that E-SSHI circuit is capable of extracting up to 5.23 and 4.02 times more power compared with an ideal full-bridge rectifier at 0.87 V and 2.6 V piezoelectric open circuit voltage amplitudes ($V_{OC,P}$), respectively. A maximum voltage flipping efficiency of 93% is observed at $V_{OC,P} = 3.6$ V, owing to minimized losses on charge flipping path. Measured results are compared with state-of-the-art interface circuits. Comparison shows that E-SSHI design offers a huge step towards miniaturized harvesting systems thanks to its low-profile and fully autonomous design.

INDEX TERMS Autonomous, low-profile, piezoelectric energy harvester, SSHI, optimal charge flipping, area efficient, IC.

I. INTRODUCTION

Downsizing in state-of-the-art and efficient wireless sensor networks (WSNs) makes them alluring for biomedical devices and many other applications where system size is a big concern [1]. Recently, power dissipation levels of such systems have been diminished thanks to advanced fabrication techniques which enable electronic circuits to support lower supply voltage levels. Still, maintaining power to portable electronic devices necessitates usage of external bulky batteries that enlarges system volume and restricts their application areas. Furthermore, batteries require continuous charging to keep electronic circuits inside WSN systems up and running for a long time. These bulky batteries with limited capacity can be removed from the system by making use of energy scavenging (i.e. energy harvesting) to power up electronic loads [1], [2]. Medical devices (health monitoring sensors, implantable pacemakers etc.), active RFID tags, and predictive maintenance could be counted as application areas for energy harvesting practices [1]. In an environment where temperature gradients and solar radiations are low, ambient vibrations are the most appealing ones owing to

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their abundance [3]. There are three main kinetic conversion principles (capacitive, inductive, and piezoelectric conversion principles) emerge for harvesting energy from vibrations or motions [4]. In centimetric or millimetric energy harvesting applications, piezoelectric energy harvesters (PEHs) are widely chosen to convert mechanical energy into electrical one thanks to their high power density and compatibility with standard CMOS fabrication processes [5]. PEH produces AC voltage of time-varying levels with excitation variations. Thus, rectification and regulation stages are needed before PEH can be utilized as a power source for WSN electronics.

During early days of PEH interface circuit design, usage of standard AC/DC rectification circuits such as full bridge rectifiers (FBRs) and voltage doublers were quite popular thanks to their simplicity [6], [7]. Yet, voltage drops on rectifier diodes hinders standard rectifiers to deliver all of generated energy on PEH to the loading circuitry. Moreover, built-in PEH capacitance needs to be charged and discharged to reach output voltage before charge transfer to the output load starts. Circuits in [8], [9] implement maximum power point tracking (MPPT) to match PEH impedance to output. However, they concentrate on matching the real parts and therefore, they lose considerable amount of energy at PEH capacitance. Nonlinear processing of piezoelectric voltage has been investigated deeply as a possible alternative solution to boost energy extraction from PEHs [3], [10]. Synchronous electric charge extraction (SECE) [5], [11]–[13] and synchronized switch harvesting on inductor (SSHI) [14]–[17] are two most common nonlinear switching techniques utilized in the literature. An external inductor is employed in SECE configuration to both decouple PEH from the system and transfer energy to output at maximum deflection of piezoelectric beam. Multi-stage energy extraction technique, published in [5], improves power conversion efficiency compared to conventional SECE circuits. To do so, it delivers load independent power through multiple energy packages, which reduces conduction losses on charging path. [11] reuses some of the charge transferred to battery as energy investment to PEH capacitance. Correspondingly, aforementioned circuit increases damping force and improves extracted output power.

Recently published SECE circuit in [13] is capable of harvesting energy from sporadic high voltage inputs thanks to its unique control circuit. Unfortunately, it contains on-chip FBR working as negative voltage converter, which hinders significant power extraction improvements. Another common nonlinear technique called SSHI utilizes an inductor to reverse the polarity of residual voltage on PEH capacitance after charging ends, and extends energy transfer duration to the battery. Output power delivered in SSHI method is unavoidably load dependent owing to the coupling between harvester and output load. Bias flip rectifier introduced in [14] offers improvement in power extraction capacity over FBRs by more than four times; however, it rectifies AC source voltage through an on-chip FBR and occupies more than 4 mm^2 chip area. The main focus of [15] is to attain a complete energy harvesting platform which integrates a conventional SSHI circuit and a MEMS harvester. Small external inductor causes poor voltage flipping efficiency, and therefore restricts power extraction improvement. SSHI rectifiers proposed in [16], [17] are both capable of scavenging energy from PEHs while incorporating maximum power point tracking (MPPT). [16] requires external calibration of sub-units to achieve MPPT, whereas perturb and observe (P&O) method employed in [17] necessitates complex control and evaluation circuits, which make both approaches hard to implement. Optimal SSHI circuit presented in [18] achieves optimum voltage flipping durations thanks to its active diodes. Unfortunately, MOSFET switches controlling energy transfer to the output load necessitate internal clock generation to determine charging interval. This clock generation demands external adjustment for different excitation frequencies and PEHs which will limit the application area. One important problem with current SECE and SSHI circuits is that they rely on bulky external inductors to reach desirable output power and power conversion efficiencies. These inductors limit application areas of energy harvesting in implantable micro-devices since they enlarge overall system volume significantly.

Lately, inductorless interfacing techniques have been proposed to shrink the size of energy harvesting systems [19]–[22]. They present a huge step towards system miniaturization. Instead of an external inductor, circuits in [19], [20] use switched capacitors (SCs) to flip residual voltage on PEH capacitance. Eight off-chip voltage flipping capacitors with matching values to PEH capacitance in [19] increase system volume. This problem is solved in flipping-capacitor rectifier (FCR) proposed in [20] which utilizes on-chip capacitors. Nevertheless, its functionality is limited to PEHs with inherent capacitance in pF range and excitation frequency around 100 kHz. Synchronized switch harvesting on capacitor (SSHC) circuit proposed recently in [21] is an advanced version of [19]. Thanks to split-electrode MEMS harvester utilized, voltage flipping capacitors are implemented on-chip. Due to significant number of switching required for voltage flipping, conversion efficiency and power extraction improvement are reduced. Besides, both SSHI [14], [16], [17] and inductorless [19]–[21] design techniques need external adjustments (i.e. calibrations) to achieve optimum voltage flipping times. Obtaining the moment of optimum voltage flipping in harvesting circuit is quite critical since this directly impacts maximum output power level.

The aim of this work is to implement an autonomous low-profile (i.e. volumes occupied by external components are small) interface circuit to extract energy from conventional PEHs. Enhanced SSHI (E-SSHI) rectification method that does not require any negative voltage converter (NVC free) is utilized to expand delivered output power in an area efficient (0.28 mm^2) chip. Unlike SSHI [14], [16], [17] and Inductorless [19]–[21] designs, optimum charge flipping times and charging intervals are detected autonomously.

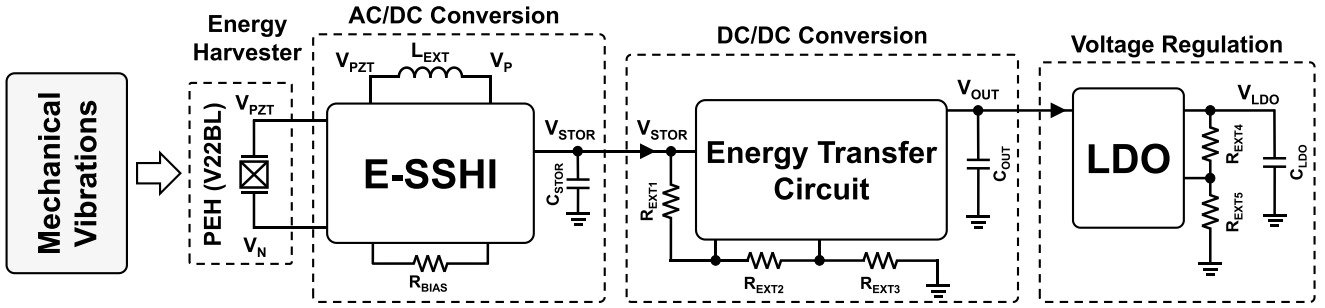

FIGURE 1. Proposed low-profile energy harvesting system.

Autonomous charge flipping and low-profile design features of E-SSHI make this system desirable in miniaturized harvesting systems. Section II provides operation principle of E-SSHI circuit and theoretical output power calculation. Implementation details of sub-units are introduced in section III. Experimental results of the fabricated ICs and performance comparison with state-of-the-art are included in section IV. Finally, section V concludes the paper.

II. ENHANCED SSHI INTERFACE CIRCUIT

Fig. 1 depicts the proposed energy harvester interfacing system. AC/DC rectification is achieved by E-SSHI circuit. It makes use of the external inductor L_{EXT} in the range of μH's to flip residual voltage on PEH capacitance and broadens the duration of storage capacitance C_{STOR} charging. Resistor R_{BIAS} helps tuning the internally generated reference voltage levels. Energy transfer circuit determines how much energy stored on C_{STOR} is delivered to output capacitance C_{OUT}. External resistors R_{EXT1}, R_{EXT2}, and R_{EXT3} provides fractions of storage voltage V_{STOR} that are needed to govern energy transfer process. Low-dropout (LDO) regulator was added for the sake of system integrity. If needed, it provides desired regulated voltage levels (lower than $VSTOR$ voltage) for electronic loads.

A. E-SSHI OPERATION PRINCIPLE

Simplified schematic of E-SSHI circuit is provided in Fig. 2. Four MOSFET switches steer current flow in the system. Equivalent circuits constructed in each operation phase is shown in Fig. 3. Initially, S_1 is the sole ON switch and upward strain on piezoelectric beam caused by ambient vibrations generates the positive charge on PEH capacitance C_{PZ} (Phase 1). During that phase, one terminal of PEH (V_N node) is connected to ground and voltage V_P increases. The moment when V_P surpasses storage voltage V_{STOR}, switch S_2 starts conducting and charge accumulation on C_{STOR} begins (Phase 2). In contrast to conventional SSHI circuits, this system does not require any negative voltage converter for battery charging purposes. Charging process ends when V_{STOR} becomes less than V_P and S_2 turns OFF. At the same time, S_3 turns ON to initiate voltage flipping on PEH capacitance C_{PZ} (Phase 3). LC resonance circuit

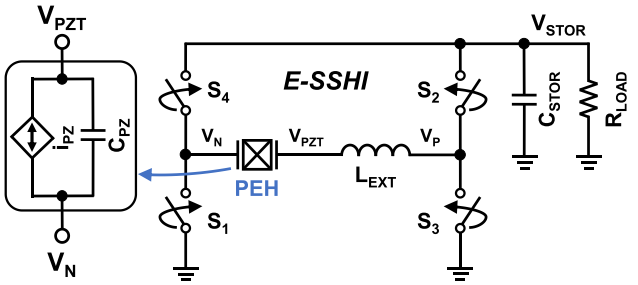

FIGURE 2. Simplified schematic of enhanced synchronized switch harvesting on inductor (E-SSHI) circuit.

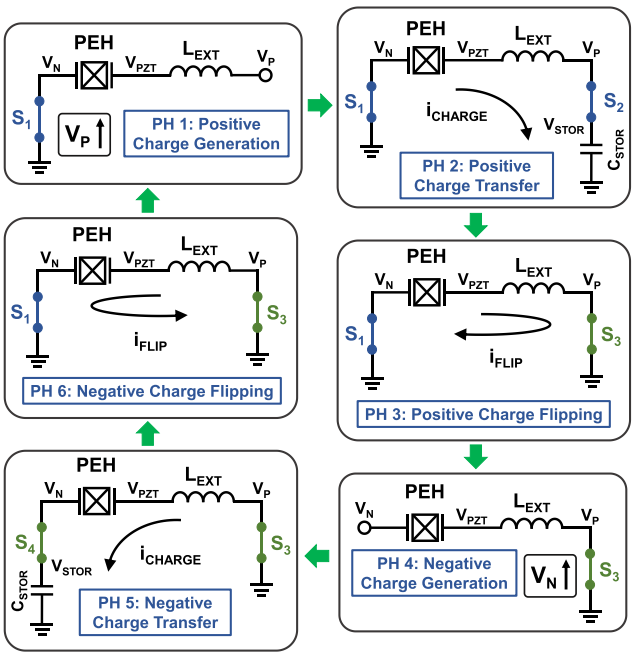

FIGURE 3. Summary of E-SSHI operation phases.

is established in order to transfer residual charge on C_{PZ} firstly to external inductor L_{EXT} and then back to C_{PZ} with reverse polarity. Voltage flipping is finalized when there is no residual charge left on L_{EXT}. Then, S_1 stops its conduction and negative charge generation is initiated (Phase 4) where voltage on node V_N rises with swinging of piezoelectric beam

(negative half cycle). Charge accumulated on C_{PZ} during negative charge generation phase is transferred through S_3 and S_4 when V_N exceeds V_{STOR} (Phase 5). When V_N recedes below V_{STOR}, S_4 is deactivated and conduction path between PEH capacitance C_{PZ} and C_{STOR} is broken. Meanwhile, system goes into the phase 6 in which S_1 is turned ON to launch negative voltage flipping on PEH capacitance C_{PZ}, just as in phase 3. When charge on L_{EXT} is depleted, voltage on C_{PZ} is reversed and system goes back into phase 1 by turning S_3 OFF. Fig. 4 depicts simulation waveforms of V_{PZT}, V_N, V_P, and inductor current i_{FLIP} observed during operation phases.

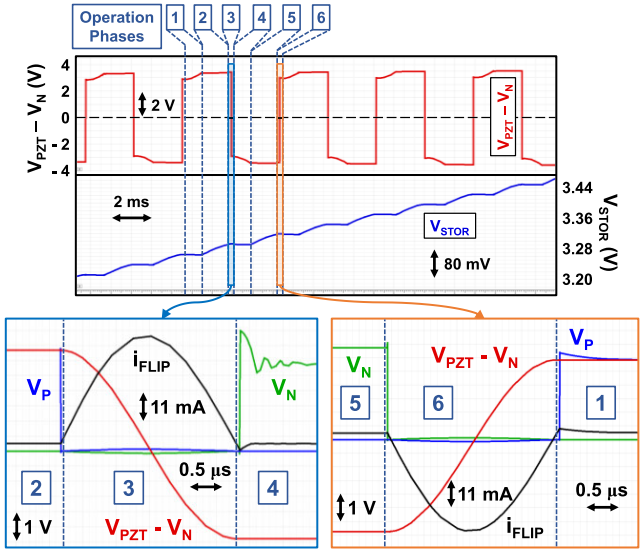

FIGURE 4. Simulation waveforms of PEH terminals V_{PZT} and V_N, inductor current i_{FLIP}, and the node V_P observed during E-SSHI operation phases.

B. OUTPUT POWER CALCULATION

PEH equivalent model parameters can be employed to express the extracted output power of E-SSHI interface circuit. Fig. 5 shows the electromechanical equivalent circuit of a piezoelectric harvester and representative waveform of voltage difference between the terminals of PEH when E-SSHI circuit is used as the interface electronics [4]. Voltage source $V_{MC} = ma/\Gamma$ represents the alternating (sinusoidal) input excitation force of the harvester (Γ is the electromechanical coupling factor, a is the acceleration, and m is the mass of the piezoelectric beam). $L_{MC} = m/\Gamma^2$ is related to effective mass, $R_{MC} = d/\Gamma^2$ represents the damping, $C_{MC} = \Gamma^2/K$ gives effect of piezoelectric stiffness K, and C_{PZ} is the inherent piezoelectric harvester capacitance [4], [23], [24]. Provided that the harvester is lowly coupled and/or highly damped, PEH model presented in Fig. 5 can be further simplified using inherent piezoelectric capacitance C_{PZ} in parallel with the current source i_{PZ} as shown in Fig. 2 [19], [23], [24].

In order to calculate theoretical harvested power of E-SSHI interface, we first assume that the circuit is at the beginning of the first phase in which electrical charge is

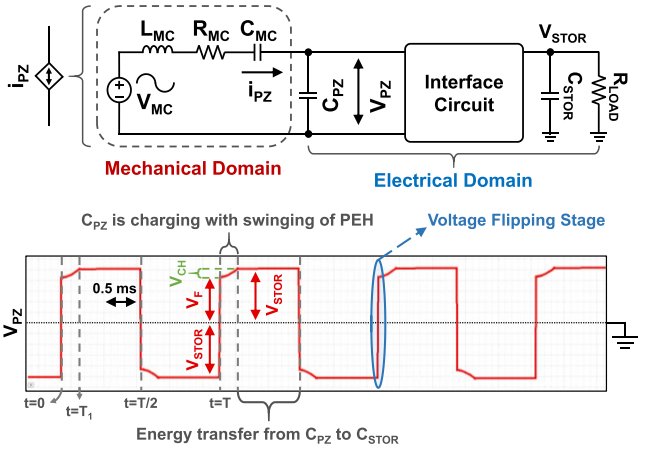

FIGURE 5. Electromechanical equivalent circuit of a piezoelectric energy harvester and representative waveform of voltage difference between the terminals of PEH (v_{PZ}) when E-SSHI circuit is used as the interface electronics.

accumulated on C_{PZ} with swinging of piezoelectric beam. Moreover, PEH is excited with its natural resonance frequency and higher harmonic terms of V_{MC} are ignored [23]. At the beginning of phase 1, which corresponds to time $t = 0$ and $t = T$ in Fig. 5, initial voltage $V_{PZ}(t = 0)$ on C_{PZ} is:

$$v_{PZ} = V_F = (2\eta_F - 1)\, V_{STOR}, \tag{1}$$

where η_F is defined as voltage flipping efficiency:

$$\eta_F = \frac{V_F + V_{STOR}}{2V_{STOR}} \Longleftrightarrow V_F = V_{STOR}\,(2\eta_F - 1)\,, \tag{2}$$

where V_F is the flipped voltage after charging. The terminal law for capacitors states:

$$i_{PZ} = C_{PZ}\frac{dv_{PZ}}{dt} \Longrightarrow i_{PZ}dt = C_{PZ}dv_{PZ}, \tag{3}$$

where $i_{PZ} = I_{PZ}\sin(\omega_N t)$, I_{PZ} is the amplitude of i_{PZ}, and $\omega_N = 2\pi/T$ is the natural resonance frequency of the PEH (PEH is excited at its resonance frequency). Assume that at $t = T_1$, V_{PZ} becomes larger than V_{STOR} and therefore, PEH starts charging C_{STOR}. This time is represented on the waveform in Fig. 5. Integration of both sides of equation (3) from $t = 0$ to $t = T_1$ results in:

$$\int_{t=0}^{T_1} I_{PZ}\sin(w_N t)dt = \int_{v_{PZ}(0)}^{v_{PZ}(T_1)} C_{PZ}dv_{PZ}, \tag{4}$$

$$-\frac{I_{PZ}}{w_N}\cos(w_N t)\Big|_{t=0}^{t=T_1} = C_{PZ}[v_{PZ}\,(T_1) - v_{PZ}\,(0)], \tag{5}$$

where $v_{PZ}(T_1) = V_{STOR}$ and $v_{PZ}(0) = V_F = V_{STOR}(2\eta_F - 1)$. Then:

$$T_1 = \frac{1}{w_N}cos^{-1}[1 - \frac{w_N}{I_{PZ}}C_{PZ}V_{STOR}2(1 - \eta_F)]. \tag{6}$$

Following the charge accumulation phase, between $t = T_1$ and $t = T/2$ (Phase 2), C_{STOR} is charged ($T = 2\pi/\omega_N$). Amount of power extracted on that phase is expressed as:

$$P_{OUT} = \frac{1}{T/2 - T_1} \int_{t=T_1}^{T/2} V_{STOR} I_{PZ} \sin(w_N t)\, dt, \tag{7}$$

under the assumption that V_{STOR} does not change much during charging. If $\eta_F > 80\%$, then approximation $T/2 - T_1 \approx T/2$ holds. Therefore:

$$P_{OUT} = \frac{2}{T} V_{STOR} I_{PZ} [-\frac{\cos(w_N t)}{w_N}]_{t=T_1}^{t=T/2}, \tag{8}$$

$$P_{OUT} = \frac{2}{T} \frac{V_{STOR} I_{PZ}}{w_N} [1 + \cos(w_N T_1)]. \tag{9}$$

Substituting for T_1 from equation (6) into (9), the following equation is derived,

$$P_{OUT} = \frac{2 V_{STOR} I_{PZ}}{\pi} - \frac{4}{T} C_{PZ} V_{STOR}^2 (1 - \eta_F), \tag{10}$$

which is exactly the same as the expression found in [23]. Furthermore, optimum storage voltage calculation was provided in detail in [23] as:

$$V_{STOR,OPT} = \frac{\pi V_{MC}}{8(1 - \frac{\pi^2}{4}[1 - \eta_F] f C_{PZ})}, \tag{11}$$

where $V_{MC} = ma/\Gamma$ and $f = 1/T$. Optimum storage voltage $V_{STOR,OPT}$ depends on PEH equivalent model parameters (C_{PZ}, Γ), input excitation of the harvester (V_{MC}, f), and interface circuit performance (η_F). Thus, to keep storage voltage level at optimum, a dedicated maximum power point tracking (MPPT) system is required which is not the focus of this study.

III. CIRCUIT IMPLEMENTATION

Fig. 6 presents implementation details of enhanced SSHI (E-SSHI) architecture. E-SSHI circuit has five sub-units. Some of E-SSHI sub-units, which are called start-up trigger circuit, reverse current detector, and voltage reference, are quite similar to the ones presented in [25]. Start-up block monitors storage voltage level V_{STOR} during cold start operation and generates a triggering signal EN_{TRIG} when sufficient charge accumulates on C_{STOR}. This signal starts E-SSHI operation phases illustrated in Fig. 3. It is important to note that during cold start, S_1 switch connects node V_N to ground and charging of C_{STOR} occurs through S_2. Reverse current detectors (RCDs) govern charging durations of output load C_{STOR} by comparing V_{STOR} with V_P and V_N. They are disabled during voltage flipping phases to reduce system's overall power consumption. Positive and negative charge flipping detectors (CFDs) check whether residual charge on external inductor L_{EXT} is transferred back to PEH capacitance C_{PZ}. In contrast to conventional SSHI [14]–[16] and inductorless designs [19]–[21], they autonomously catch moments of optimum energy transfer from L_{EXT} to C_{PZ} in charge flipping

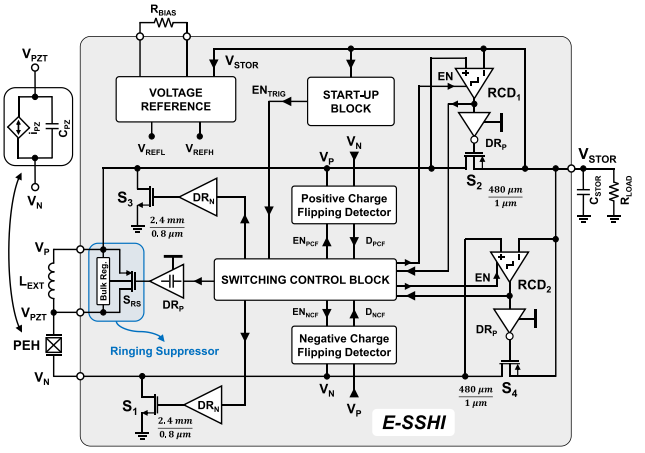

FIGURE 6. System architecture of enhanced synchronized switch harvesting on inductor (E-SSHI) circuit.

phases (Phases 3 and 6) and communicate with switching control block using D_{PCF} and D_{NCF} signals. Switching control block, which makes use of control signals generated internally, is composed of various digital logic gates and SR latches. It determines ON and OFF durations of switches S_1-S_4 and produces enable signals of other sub-units. These enabling signals help system to minimize its energy consumption. On-chip voltage reference circuit creates two stable voltage levels which are employed as biasing references in E-SSHI system. Biasing voltage levels can be tuned externally via R_{BIAS}. Sub-units inside E-SSHI use V_{STOR} voltage as their supply voltage V_{DD} (E-SSHI is a self-powered system).

A. START-UP TRIGGER

E-SSHI circuit is capable of cold start-up operation. Thanks to S_1 and S_2, load capacitor C_{STOR} is charged passively during start-up, which does not demand usage of a negative voltage converter (NVC), unlike the scheme used in [16]. When V_{STOR} hits around 1.2 V, RCDs and SR latches in switching control block are enabled to sequence E-SSHI phases. This sequencing is initiated by the start-up trigger circuit which is illustrated in Fig. 7.

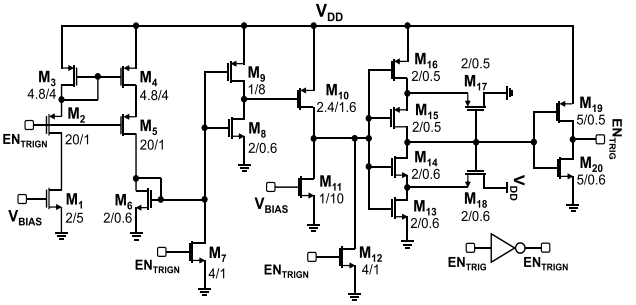

FIGURE 7. Schematic of start-up trigger circuit.

Bias voltage levels develop at the gates of transistors M_1 and M_{11} during startup, while V_{DD} also builds up. The current through M_1 is mirrored through M_3-M_4-M_6 and charge is

collected at M_8 and M_9 gates. Accumulated charge on the gates in a specific period can be adjusted using V_{BIAS} voltage. M_8 and M_9 form an inverter that triggers generation of EN_{TRIG} signal, which in turn enables E-SSHI phases. Start-up trigger is deactivated entirely after the generation of EN_{TRIG} signal.

B. REVERSE CURRENT DETECTORS

E-SSHI circuit is capable of cold Autonomy in E-SSHI switching is secured by a set of reverse current detectors (RCDs) and charge flipping detectors (CFSs) which work in harmony. There exist two RCDs (RCD_1 and RCD_2) that are responsible for regulating C_{STOR} (i.e. battery) charging duration in the course of positive and negative half cycles of piezoelectric motion. RCD circuit depicted in Fig. 8(a) benefits from a hybrid 2-stage comparator topology. Besides conventional differential input pair of M_9-M_{10}, transistors M_{11} and M_{12} form common gate configuration to facilitate detection sensitivity of the instant when V_+ first drops below V_- ($V_{DD} = V_{STOR}$). Both RCDs are active for almost full duration of the piezoelectric half cycles. Therefore, their power dissipation levels have utmost importance on system efficiency. M_{20} functions as a current limiter which curtails current drawn from supply voltage during RCD output transitions. Fig. 8(b) shows simulation waveforms of control signal generated by RCDs and CFDs. The waveform of C_{STOR} charging current, i_{CHARGE}, is also provided in the same figure.

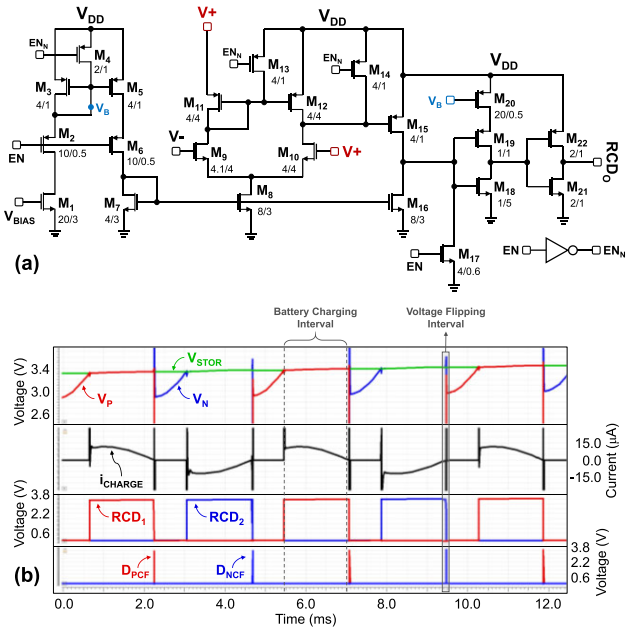

FIGURE 8. (a) Schematic of reverse current detector (RCD) and (b) its simulation result showing generated control signals of both RCDs and charge flipping detectors (CFDs).

C. CHARGE FLIPPING DETECTORS

The charge flipping sensors detect whether the current on the external inductor is depleted or not. Charge flipping action is accomplished when all current generated on the inductor L_{EXT} flows back into the piezoelectric capacitance C_{PZ}. The structure presented in Fig. 9(a) senses the depletion point by monitoring voltage drops on S_1 and S_3. While the current on L_{EXT} flows into C_{PZ}, sign change of voltage drops on switches indicates the end of charge flipping action.

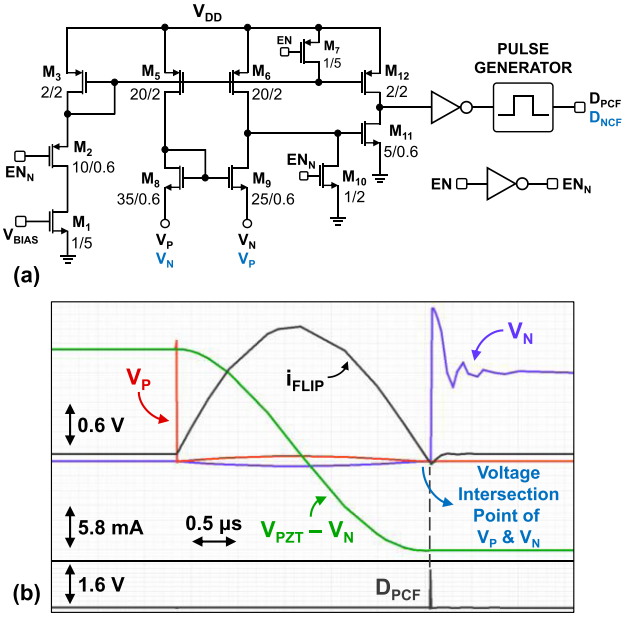

FIGURE 9. (a) Schematic of charge flipping detector (CFD) and (b) its simulation result indicating node voltage V_P, V_N, flipping current i_{FLIP}, and detection signal D_{PCF}.

A current follower input stage monitoring switch voltage drops is followed by a common source amplifier and together they form the comparator as shown in Fig. 9(a). The transistor sizes are determined to provide required gain within subthreshold biasing region. An offset is imposed by slightly mismatching the aspect ratio of M_8 and M_9 MOSFETs to avoid premature switching during transition. Mismatch is adjusted at differential stage through simulations to achieve 20 mV offset. High outputs of CFDs warn the system about the fact that inductor does not store any energy inside. Fig. 9(b) depicts simulation waveforms of V_P, V_N, i_{FLIP} and detection signal D_{PCF} observed in flipping action.

D. VOLTAGE REFERENCE

Biasing of E-SSHI sub-units is accomplished by the voltage reference circuit shown in Fig. 10(a). This is the modified version of PTAT bias-current generator designed in [11]. Gate-source voltage difference between M_1 and M_2 transistors builds a voltage drop on resistor R_{BIAS}. NMOS transistors M_3 and M_4 balance the bias current through M_1 and M_2. This supply independent current is mirrored through M_5 and M_8 and is then converted into reference voltage levels using NMOS saturated load transistors M_6, M_7, and M_9. M_{S1}-M_{S5} and C_S serve as start-up configuration. Generated reference

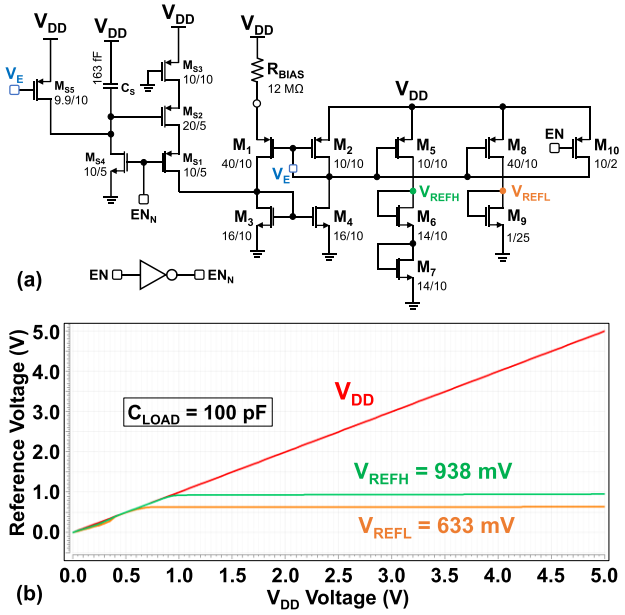

FIGURE 10. (a) Voltage reference circuit and (b) its corresponding simulation waveforms under changing supply voltage levels.

levels V_{REFH} and V_{REFL}, whose simulation waveforms are provided against V_{DD} in Fig. 10(b), can be tuned via R_{BIAS}.

E. ENERGY TRANSFER CIRCUIT

Amount of energy stored on C_{STOR} (i.e. E-SSHI output) can be delivered to C_{OUT} through energy transfer circuit (ETC) depicted in Fig. 11. As stated in output power calculation section, optimum storage voltage $V_{STOR,OPT}$ is contingent upon both PEH parameters and interface circuit performance. ETC is capable of providing controllable energy transfer in accordance with predetermined voltage threshold levels V_{P1} and V_{P2} to keep V_{STOR} near its optimum value. These thresholds are adjusted with external resistors R_{EXT1}, R_{EXT2}, and R_{EXT3}. ETC allows V_{STOR} to obtain voltage levels in the range:

$$\frac{R_{TOTAL}}{R_{EXT2}+R_{EXT3}}V_{PM} > V_{STOR} > \frac{R_{TOTAL}}{R_{EXT3}}V_{PM}, \quad (12)$$

where $R_{TOTAL} = R_{EXT1} + R_{EXT2} + R_{EXT3}$, and V_{PM} is internally generated reference voltage connected to V_{REFH} in Fig. 10(a). Hysteresis comparators inside ETC continuously monitor threshold voltage levels against V_{PM} and generate controls for the SR-latch. An external enable switch activates ETC when needed. Along with the condition specified in equation (12), V_{STOR} must be higher than V_{OUT} to transfer energy from C_{STOR} to C_{OUT}. Switch MOSFET S_5 prevents energy leakage from C_{OUT}.

IV. MEASUREMENT RESULTS

Proposed harvesting interface system is designed and fabricated in 180 nm CMOS technology with total of 0.28 mm^2 active area. Die micrograph of the fabricated chip is shown in Fig. 12. E-SSHI circuit occupies 300 × 400 μm^2

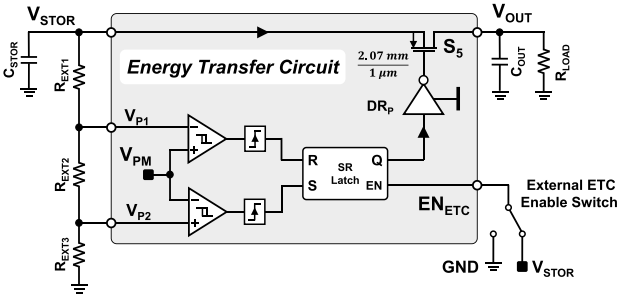

FIGURE 11. Energy transfer circuit (ETC) architecture.

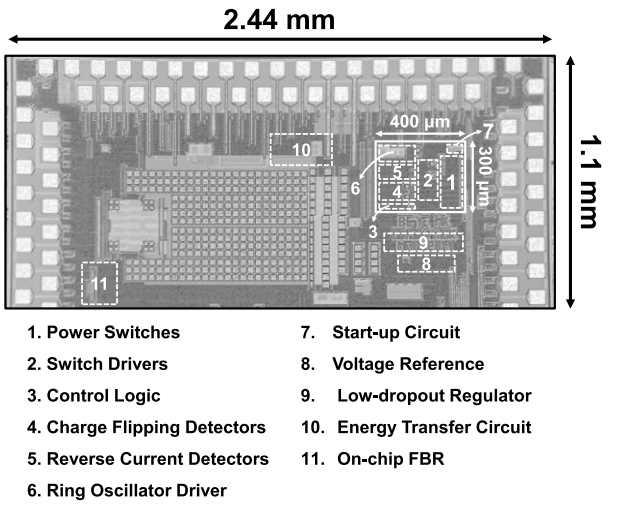

FIGURE 12. Die micrograph of the proposed harvesting interface fabricated in 180 nm CMOS technology.

whereas voltage reference takes up 230 × 50 μm^2. Low-dropout (LDO) regulator and ETC use 500 × 56 μm^2 and 270 × 110 μm^2, respectively. Fig. 13 illustrates the experimental setup employed to validate the fabricated chips. A conventional piezoelectric harvester V22BL from MIDE company with 4.66 nF inherent capacitance (C_{PZ}) has been set onto a shaker table. This harvester included two electrically detached piezoelectric layers which were connected in series to enhance PEH voltage output during the experiments. PEH was excited periodically at 208 Hz resonance frequency in the vibration setup, which comprised of a test PCB, a shaker table, an amplifier, a controller, vibration software, and an oscilloscope. Acceleration of the shaker table was selected between 0.13 g and 0.53 g which corresponded to piezoelectric open circuit voltage amplitudes ($V_{OC,P}$) of 0.87 V and 3.6 V, respectively. Five SMD inductors with inductances 68 μH (R_{DC} = 3.86 Ω), 330 μH (R_{DC} = 1.93 Ω), 470 μH (R_{DC} = 1.35 Ω), 680 μH (R_{DC} = 2.02 Ω), and 820 μH (R_{DC} = 2.53 Ω) have been utilized as L_{EXT} for voltage flipping purposes.

Measured start-up operation is presented in Fig. 14. During start-up, C_{STOR} = 449 nF is charged passively through S_1 and S_2. Trigger circuit in Fig. 7 initiates E-SSHI phases

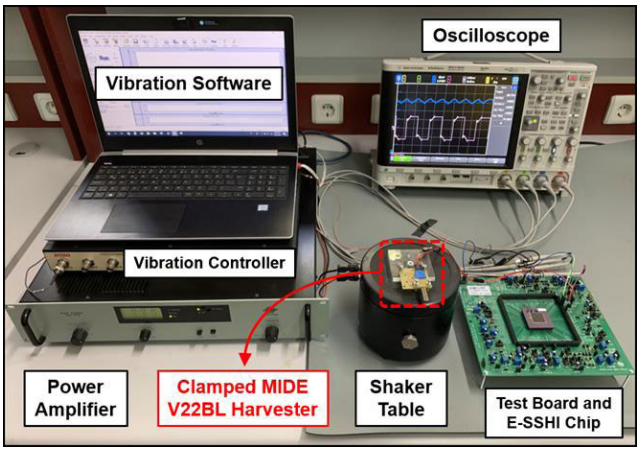

FIGURE 13. Experimental setup employed for performance evaluation of fabricated E-SSHI chips.

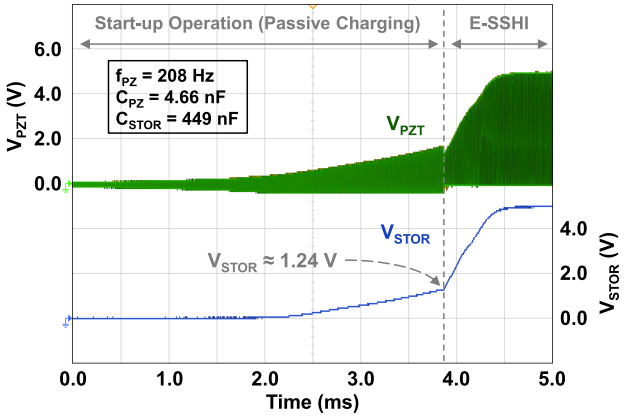

FIGURE 14. Measured waveforms of piezoelectric voltage V_{PZT} and storage voltage V_{STOR} during start-up operation.

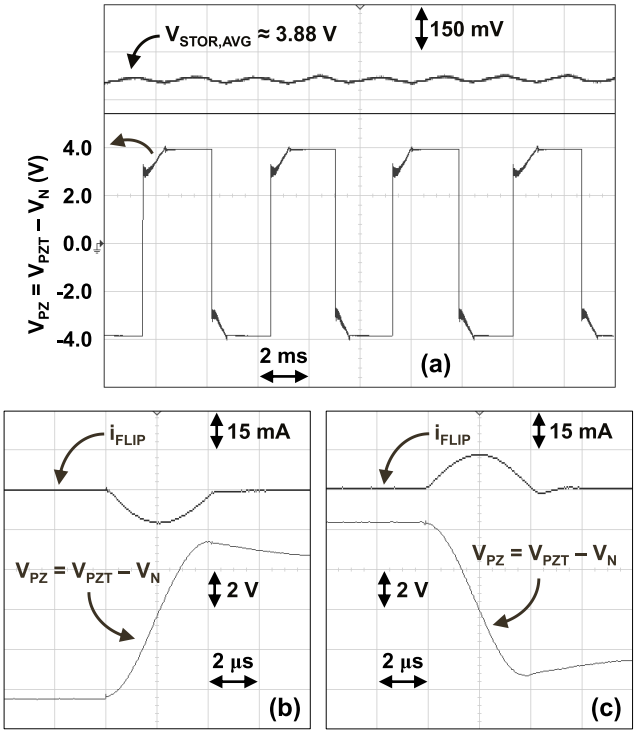

FIGURE 15. Measured waveforms of voltage difference between PEH terminals V_{PZ}, storage voltage V_{STOR}, and inductor current i_{FLIP} demonstrating (a) C_{STOR} charging, (b) negative, and (c) positive charge flipping operations in E-SSHI.

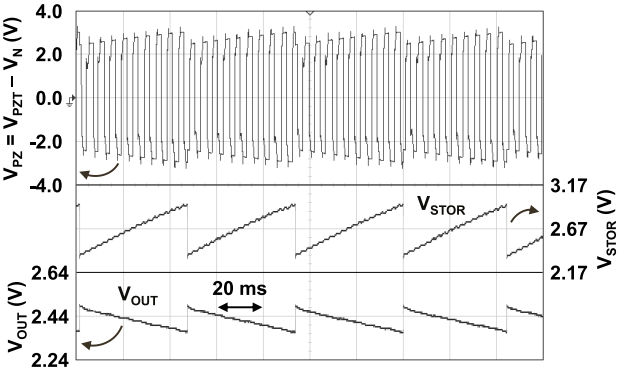

FIGURE 16. Measured waveforms of voltage difference between PEH terminals V_{PZ}, storage voltage V_{STOR}, and energy transfer circuit (ETC) output voltage V_{OUT} demonstrating verification of ETC operation.

when adequate charge accumulates on C_{STOR}. This voltage level corresponds to $V_{STOR} = 1.24$ V in Fig. 14. NVC free E-SSHI operation accelerates charging of C_{STOR} significantly compared to passive charging. Fig. 15(a) depicts measured charging of C_{STOR} with E-SSHI technique while Fig. 15(b) and 15(c) illustrate negative and positive voltage flipping operations, respectively. CFDs inside E-SSHI make it possible to attain optimum charge flipping without any external calibration. The system utilizes low-profile external inductors to obtain similar voltage flipping efficiency to conventional SSHI circuits with bulky external components [14], [17], [23]. Validation of energy transfer circuit (ETC) operation is depicted in Fig. 16. ETC regulates average V_{STOR} to be about its optimum value $V_{STOR,OPT} \approx 2.68$ V for peak piezoelectric open circuit voltage of 1.31 V, while transferring energy from $C_{STOR} = 449$ nF to $C_{OUT} = 2.2$ μF. Maximum and minimum voltage levels that V_{STOR} can take is alterable via external resistors R_{EXT1}, R_{EXT2}, and R_{EXT3} in Fig. 11.

Fig. 17 and Fig. 18 provide measured output power of E-SSHI operation under $V_{OC,P} = 0.87$ V and $V_{OC,P} = 2.6$ V peak piezoelectric open circuit voltage excitation levels, respectively. While $L_{EXT} = 820$ μH is utilized, E-SSHI circuit is able to deliver a maximum of 3.84 μW power to the load whereas on-chip full bridge rectifier (FBR) provides 0.62 μW and ideal FBR can theoretically output a maximum of 0.734 μW. Ideal FBR can be delineated as a rectifier (without voltage drop across its diodes) which is able to provide theoretical maximum output power of $P_{IDEAL-FBR} = f_{EX} C_{PZ} V_{OC,P}^2$ [11], [14]. Fig. 17 illustrates that E-SSHI realizes 5.23 and 6.19 times relative output

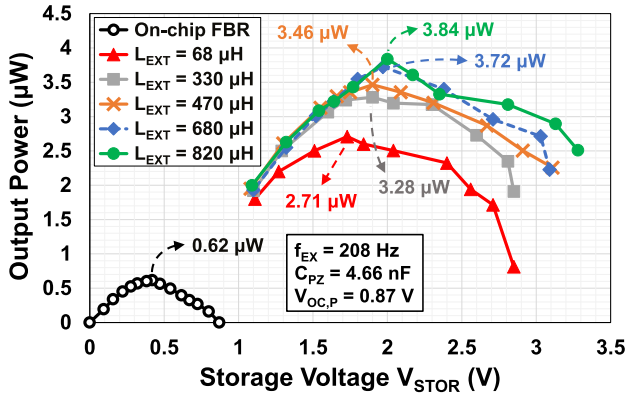

FIGURE 17. Measured output power of E-SSHI circuit versus storage voltage V_{STOR} for $V_{OC,P}$ = 0.87 V.

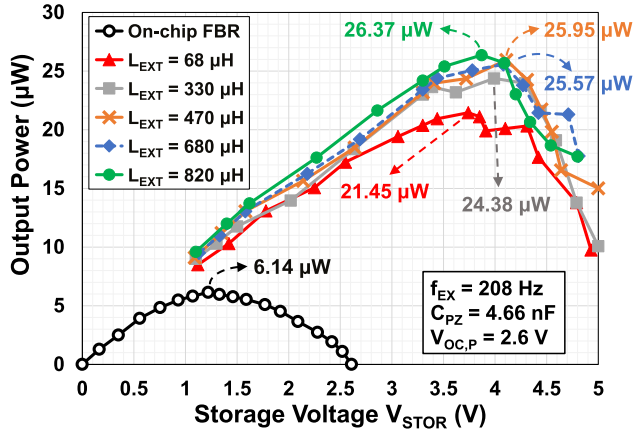

FIGURE 18. Measured output power of E-SSHI circuit versus storage voltage V_{STOR} for $V_{OC,P}$ = 2.6 V.

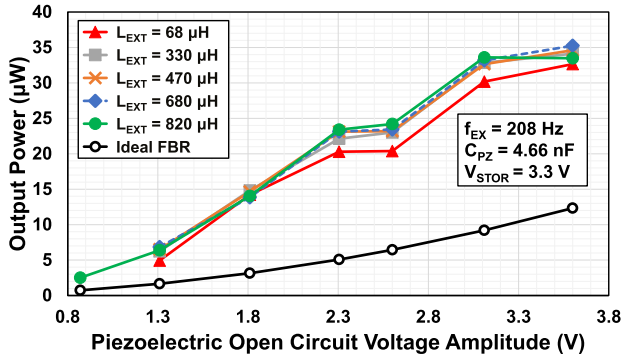

FIGURE 19. Measured output power of E-SSHI circuit under various piezoelectric excitation levels ($V_{OC,P}$) while V_{STOR} = 3.3 V.

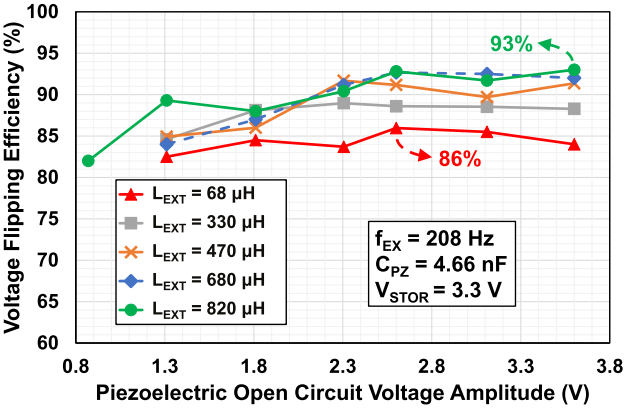

FIGURE 20. Measured voltage flipping efficiencies (η_F) under various piezoelectric excitation levels ($V_{OC,P}$) while V_{STOR} = 3.3 V.

power performance over harvested power of an ideal FBR and on-chip FBR, respectively. It is possible to shrink L_{EXT} inductance value down to 68 μH, which has small footprint (18 mm^3), in exchange for reduction in power extraction improvement. Relative power extraction improvement reduces while piezoelectric open circuit voltage increases, because damping of PEH strengthens with increased excitation levels (Fig. 18) [26]. Under high excitation, interface circuit suffers from elevated conduction and switching losses. Fig. 19 depicts output power of E-SSHI circuit under various excitation conditions while V_{STOR} is kept constant at 3.3 V. As observed in the plot, increased external inductance does not always enhance output power. Each inductor offers different voltage flipping efficiency, which leads to different optimum storage voltage value ($V_{STOR,OPT}$). Measured voltage flipping efficiencies (η_F) under different excitations are plotted in Fig. 20. Maximum η_F = 93% is observed for L_{EXT} = 820 μH at $V_{OC,P}$ = 3.6 V. Even when L_{EXT} is decreased down to 68 μH, E-SSHI still manages to grant maximum η_F of 86% recorded at $V_{OC,P}$ = 2.6 V.

Table 1 presents a performance comparison of E-SSHI proposed in this work against state-of-the-art PEH interface circuits in the literature. E-SSHI stands out among its peers in terms of fully autonomous charge flipping and area efficient design. Furthermore, it achieves flipping efficiencies comparable to conventional SSHI circuits [15]–[17] even with low-profile inductors under 1 mH. SECE based interface circuit in [12] was designed specifically for shock type excitations and its performance under periodic excitations is inferior with respect to E-SSHI. Recently, partial electric charge extraction (PECE) technique similar to SECE has been proposed in [13]. It focuses on extracting energy from PEH generating irregular high voltage outputs. In this circuit, AC/DC conversion was attained using conventional off-chip FBR that limited power extraction improvement. Circuit in [16] employed a bulky external inductor to accomplish a conventional SSHI interface that is able to extract energy from both periodic and shock excitations; however, it is not convenient for a miniaturized systems. Perturb and observe (P&O) maximum power point tracking (MPPT) method was integrated inside a conventional SSHI by Li *et al.* [17]. A complex control unit was required in this design and measured performance parameters fall behind E-SSHI circuit presented in this work. Peng [24] proposed a novel harvesting

TABLE 1. Comparison of the implemented IC with state-of-the-art.

Ref.	C_{PZ}	$V_{OC,P}$	f_{EX}	Inductor (Volume)	Flipping Time Detection	Cold Start	Peak Voltage Flipping Efficiency	Chip Size	Power Extraction Improvement (FOM(1)x100)
[12] SECE	43 nF	NA	75.4 Hz	2.2 mH (0.13 cm^3)	NA	YES	NA	0.55 mm^2	314%
[13] PECE	20 nF	55 V	NA	220 µH (NA)	NA	NO	NA	3.51 mm^2	390(2)%
[16] SSHI	9 nF	0.95 V	229 Hz	3.3 mH (15.2 cm^3)	External Adjustment	YES	94%	1.17 mm^2	440%
[17] SSHI	20 nF	1.6 V	100 Hz 180 Hz	3.3 mH (NA)	External Adjustment	YES	86%	1.07 mm^2	417%
[24] SaS	8 nF	0.95 V	85 Hz 53 Hz	1 mH (NA)	NA	YES	NA	0.47 mm^2	541%
[20] FCR	80 pF	NA	110 kHz	NO	External Adjustment	YES	85%	1.70 mm^2	483(2)%
[21] SE-SSHC	1.94 nF	2.5 V	219 Hz	NO	External Adjustment	NO	85.6(3)%	3.90 mm^2	606(3)%
This Work (E-SSHI)	**4.66 nF**	**0.87 V**	**208 Hz**	**68 µH (18 mm^3) 330 µH (83 mm^3) 470 µH (151 mm^3) 680 µH (82 mm^3) 820 µH (245 mm^3)**	**Autonomous Adjustment**	**YES**	**86% (68 µH) 89% (330 µH) 91.7% (470 µH) 92.7% (680 µH) 93% (820 µH)**	**0.28 mm^2**	**369% (68 µH) 447% (330 µH) 471% (470 µH) 507% (680 µH) 523% (820 µH)**

(1) FOM = $P_{STOR}/f_{EX}V_{OC,P}^2C_{PZ}$ (2) Calculated with respect to on-chip FBR. (3) Calculated from paper.

interface called sense-and-set (SaS) rectifier which continuously monitors PEH's charge generation and tries to keep battery voltage at optimum. Due to technology limitation, SaS circuit stops tracking optimum point after battery voltage passes 2 V. In addition, 1 mH external inductor increases system volume. Inductorless designs presented in [20], [21] integrates flipping capacitors on-chip which is a huge step towards miniaturization. Nonetheless, both interface circuits were designed for particular applications and harvesters: Flipping-capacitor rectifier (FCR) in [20] works with PEH inherent capacitances in pF range, and split-electrode synchronized switch harvesting on capacitor (SE-SSHC) utilizes custom MEMS harvester having four identical electrodes with equal C_{PZ}'s and resonance frequencies. Area efficient E-SSHI circuit's ability to operate with low-profile external inductor reduces system volume and cost and leads the way towards miniaturization. Unlike conventional SSHI methods and inductorless designs, autonomous operation phases eliminate external intervention for obtaining optimum voltage flipping moments.

V. CONCLUSION

In this paper, an autonomous low-profile SSHI based piezoelectric energy harvesting interface circuit has been proposed. Both optimum voltage flipping and energy transfer to the output load have been achieved autonomously by charge flipping and reverse current detectors. Since E-SSHI does not contain any negative voltage converter, it occupies less chip area than its counterparts. Energy transfer circuit is capable of transferring energy from E-SSHI output to electronic load to keep storage voltage at its optimum value. Proposed harvesting interface has been fabricated in 180 nm CMOS process and occupies 0.28 mm^2, which is smaller than other circuits in the literature. A maximum of 5.23 times relative performance improvement over ideal FBR is achieved by E-SSHI circuit. 93% voltage flipping efficiency has been measured for low-profile $L_{EXT} = 820\ \mu$H at $V_{OC,P} = 3.6$ V. This work exhibits power improvement over conventional methods and offers a compact harvesting system for PEHs with several nF capacitance range.

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