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Fully Integrated Ultra-Low Voltage Step-up Converter with Voltage Doubling LC-Tank for Energy Harvesting Applications

H M P C Jayaweera[1], W P M R Pathirana[1], Ali Muhtaroğlu[1,2]

[1]Sustainable Environment and Energy Systems
[2]Dept. of Electrical-Electronics Engineering
Middle East Technical University Northern Cyprus Campus
Kalkanli, Guzelyurt, Mersin 10, Turkey

E-mail: {pradeep.jayaweera, manula.pathirana, amuhtar}@metu.edu.tr

Abstract. This paper reports the design, fabrication, and validation of a novel integrated interface circuit for ultra-low voltage step up converter in 0.18 µm CMOS technology. The circuit does not use off-chip components. Fully integrated centre-tap differential inductors are introduced in the proposed LC oscillator design to achieve 38% area reduction compared to the use of four separate inductors. The efficiency of the system is hence enhanced through the elimination of clock buffer circuits traditionally utilized to drive the step-up converter. The experimental results prove that the system can self-start, and step 0.25 V up to 1.7 V to supply a 46 µW load with 15.5% efficiency. The minimum validated input voltage is 0.15 V, which is boosted up to 1.2 V under open circuit conditions.

1. Introduction

Due to recent developments in remote and embedded microsystems working with only micro- to milli-Watts of power, energy harvesting micro-power generators have become key enablers in electronic industry. However, small micro-power generators used to harvest energy from the ambient environment are limited in capacity. DC-DC boost converters are necessary to attain a sufficiently high voltage from ultra-low voltage output of the energy harvesters, such as thermoelectric micro-modules used in wearable computing. Charge-pumps have been commonly used in such miniaturized applications, for which on-chip integration of step-up circuits is a critical system design requirement.

Typical requirements from on-chip charge-pumps include maximized efficiency to enable more features at the load, self-starting operation with minimum or no external component support, and ultra-low input voltage range (~200 mV) – often much lower than the threshold voltage of the low cost MOSFET technologies [1] [2]. Most of the integrated charge-pumps utilized in memories, liquid crystal display drivers and control systems for motor drivers consist of non-inductive circuits [3]. Inefficiency of on-chip inductors is often perceived as an inhibitive design problem. Hence, conventional clock generator circuits, such as the ones presented in [4] and [5], employ ring oscillators with buffer circuits in the final stage to sustain edge rates and high drive currents required to switch the charge-pump capacitors. However, dynamic power consumed by large CMOS clock buffers can be a significant portion of the total power budget available from micro-power generators.

In this paper, validation data from an alternative clock generator design is presented. The circuit replaces digital oscillators with a low cost voltage-doubling LC tank implemented in standard 0.18 µm CMOS technology with on-chip inductors, eliminates large CMOS buffers, and thus provides high step-up ratio at higher efficiency and larger output power capacity compared to the alternatives. The resulting step-up converter, illustrated in Fig. 1, is capable of self-starting, and boosting an input voltage as low as 0.15 V. Section 2 presents the design and analysis of the clock generation circuit. The charge-pump design, also utilized in a number of previous designs, is briefly introduced in Section 3. Experimental results from the test chip under targeted load conditions are provided in Section 4. Finally, Section 5 highlights conclusions from this work.

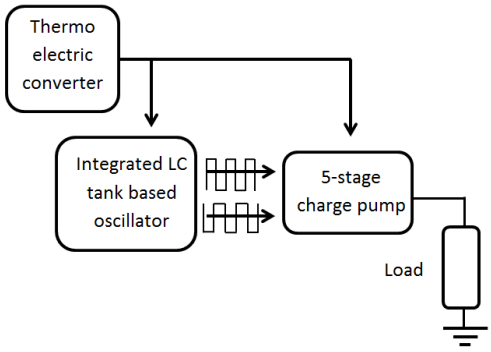

Figure 1. Block diagram of the proposed system.

2. Clock Generation Circuit

The clock generator is required to operate with an ultra-low voltage supply in a self-starting, efficient mode to provide two out-of-phase clock signals. Use of digital CMOS buffers in conventional ring oscillators increases dynamic power dissipation, and reduces efficiency. LC oscillators, which are more suitable for out-of-phase differential clock generation, have traditionally been avoided due to potentially high cost associated with on-chip inductor design. In this work an LC tank [10] based oscillator topology was enhanced, and implemented in standard (low cost) 180 nm CMOS technology. The circuit model for the LC tank based oscillator is depicted in Fig. 2(a). R_p is the parasitic resistance of the LC tank, and $-R_a$ is the negative resistance used to compensate R_p, in order to generate an undamped system. The cross-coupled NMOS pair; shown in Fig. 2(b) provides the negative resistance ($-R_a$) for the LC tank as describe in [10].

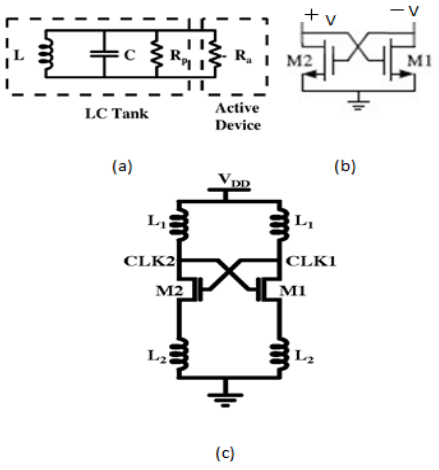

Figure 2. (a) Schematic of LC oscillator, (b) Cross coupled NMOS pair, (c) LC tank based oscillator

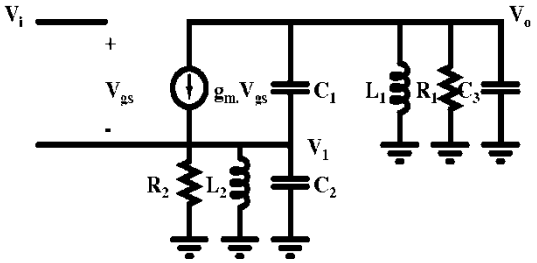

Figure 3. Half circuit model of the oscillator.

The frequency of the proposed LC oscillator is given by Equation (1):

$$f_0 = \frac{1}{2\pi\,(LC)^{1/2}} \tag{1}$$

where f_0 is the frequency of the LC tank based oscillator, C (C_{tank}) is the parasitic capacitance of the NMOS M1 and M2, and L (L_{tank}) is the inductance of the inductor shown in Fig. 2(c). The circuit parameters can calculate using the transient analysis for the half circuit model as shown in Fig. 3. According to the Kirchhoff's low, the current at node V1 can written as,

$$\frac{V_1}{R_2} + \frac{V_1}{L_2 s} + V_1 C_2 s - (V_2 - V_1) C_1 s = g_m V_{gs} \tag{2}$$

$$\frac{V_0}{L_1 s} + \frac{V_0}{R_1} + V_0 C_3 s - (V_1 - V_0) C_1 s = -g_m V_{gs} \tag{3}$$

By asserting V_0/V_i = -1 (Barkhausen criteria) to sustain oscillation, and considering the real part, the final equation can derive as follows:

$$a\omega^4 + b\omega^2 + c = 0 \tag{4}$$

where,

$$a = (C_1 L_1 R_1)(C_2 L_2 R_2) + (C_3 L_1 R_1)(C_2 L_2 R_2) + L_2 R_2 L_1 R_1 C_1 C_3$$

$$b = -(C_3 L_1 R_1 R_2 + L_1 L_2 + C_2 L_2 R_2 R_1 - g_m L_1 R_1 L_2 + C_1 L_1 R_1 R_2 + g_m L_1 R_2 L_2 + C$$

$$c = R_2 R_1$$

The inductors L_1 and L_2 are implemented as two center tap differential inductors to minimize the cost and chip area. To obtain 1 GHz frequency for the ultra-low voltage range, the inductances are selected as L_1=15 nH and L_2 = 1.6 nH. The quality factor and self-resistance of the inductor L1 are 5.8, 13.6 Ω, and L2 inductor is 3.5, 2.96 Ω respectively. The spiral Inductor Assistant software for Sonnet is used to design the layout of the inductor and 3D planner electromagnetic field solver software is used to model the inductor. The inductors are designed using UMC 0.18µm CMOS technology with 19 µm wide and 20KA Aluminum top Metal 6 and Metal 5 layers in order to generate relatively high quality factor values. The total area for the center-tap differential inductors is 0.61 mm^2. R_2 and C_2 are the parasitic resistance and capacitance of L_2. R_1 and C_3 are the parasitic resistance and capacitance of L_1. C_1 is the parasitic capacitance of the NMOS. For the clock frequency range of 1 GHz, R_1 is around 2240 Ω and R_2 is 77 Ω. The calculated transconductance of the NMOS is approximately 5 mA/V. C_1, C_2 and C_3 values are 100 fF, 0.4 pF, and 1.68 pF respectively. The oscillation frequency is derived as:

$$f_o = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{15 \times 10^{-9} \times 1.68 \times 10^{-12}}} = 1GHz$$

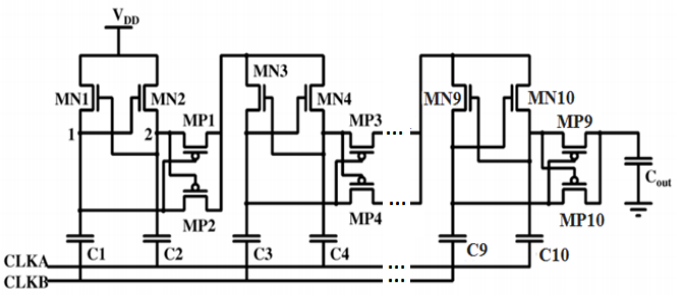

Figure 4. Charge-pump circuit with cross connected NMOS[9]

3. Charge-Pump Circuit

Dickson charge-pump [6] and its derivatives [7], [8] are commonly used for on-chip voltage step-up. An ultra-low voltage derivative was proposed by [9] as shown in Fig. 4. A five stage version of this design has been implemented in this work with suitable MOSFET parameters to minimize power dissipation and current backflow. Further details on the operation of this design can be found in [9].

4. Experimental Results

The system has been designed in UMC 0.18µm CMOS technology, and SONNET 3D Planner Electromagnetic Field Solver Software is used to characterize the centre tap inductors for the LC tank based oscillator. The circuit with LDO regulation stage occupies 0.88 mm^2 of layout area, although regulation mode has not been utilized in this work. The full chip layout of the step-up converter is shown in Fig. 5.

The fabricated charge-pump design has been validated using 30 pF capacitive load and various load resistance values. The measured system efficiency curve is depicted in Fig. 6 against varying load resistance with 0.25 V input. The maximum efficiency is achieved for a load resistance of 60 kΩ. The proposed system can convert 0.25 V to 1.1 V with 30 kΩ load resistance, as depicted in Fig. 7. For 60 kΩ load resistance, the system can achieve 1 V output level at 0.2 V input, as shown in Fig. 8. The experimental results demonstrate the system can self-start, and step 0.25 V up to 1.7 V to supply a 46 µW load with 15.5% efficiency. The minimum validated input voltage is 0.15 V, which is boosted up to 1.2 V under open circuit conditions. At ultra-low voltage range, the proposed step-up converter is smaller in size, and has higher integration with improved efficiency compared to the alternatives [11], [12], [13] respectively in 0.18 µm technology.

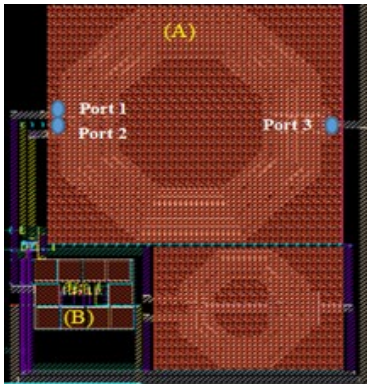

Figure 5. Die layout of the fabricated system.

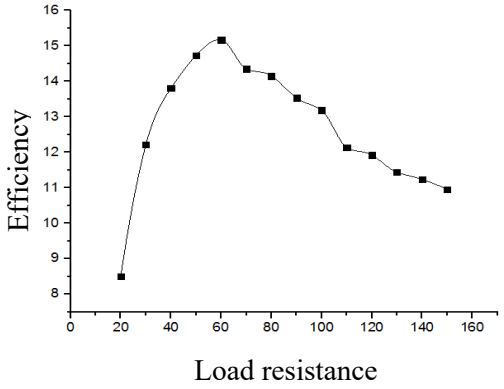

Figure 6. System Efficiency vs. load resistance for 0.25 V input voltage.

5. Conclusion

An ultra-low voltage step-up integrated charge-pump circuit topology with voltage doubling LC tank for interfacing micro-power generators has been designed, fabricated, and validated using 0.18µm standard CMOS technology, with 0.88 mm^2 area. The center tap differential inductors in the LC tank achieve 38% area saving compared to the usage of four distinct inductors. The system can self-start as low as 0.15 V, and generate an out-of-phase clock pair with amplitude 0.30 V at this input voltage. 0.25 V can be stepped up to 1.7 V with input load resistance of 60 kΩ and maximum efficiency of 15.5%. Therefore, a step-up ratio of 1:6.8 is achieved at highest efficiency. At 160 kΩ load resistance and 0.25 V input, the effective step-up ratio increases to 1:9.

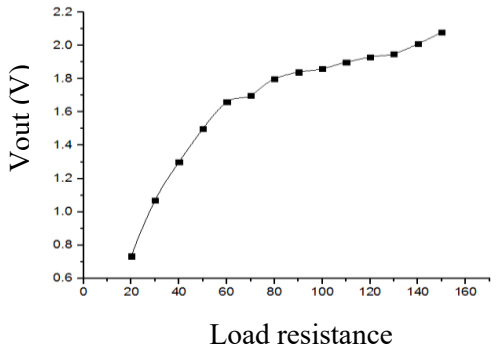

Figure 7. System unregulated output voltage with varying load resistance for 0.25 V input voltage.

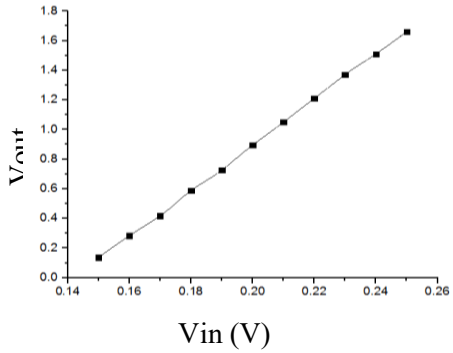

Figure 8. The variation of output voltage with input voltage for 60 kΩ load resistance.

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